PATENT APPLICATION
Do. No. 4591-183

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jae-Hak KIM, et al.

Serial No. 09/919,340 Examiner: Erdem, Fazli

Filed: July 30, 2001 Group Art Unit: 2826

For: **METHOD FOR FABRICATING SEMICONDUCTOR DEVICE CAPABLE OF REDUCING PARASITIC CAPACITANCE AND SEMICONDUCTOR DEVICE THEREBY**

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents,
Washington, D.C. 20231

Responsive to the Office Action dated June 20, 2002, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	15	11	0	x $18 =	$0
Independent Claims	3	2	0	x $84 =	$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$0

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

20575
PATENT TRADEMARK OFFICE

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I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO COMMISSIONER OF PATENTS & TRADEMARKS WASHINGTON D.C. 20231 OR ASSISTANT COMMISSIONER FOR TRADEMARKS 2900 CRYSTAL DR ARLINGTON VA 22202-3513
ON 9-19-02

#6 Amdt. A 10/2/02

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RESPONSE TO OFFICE ACTION

Responsive to the Office Action, dated June 20, 2002, please amend the application as follows.

IN THE SPECIFICATION

Replace the paragraph beginning at page 1, line 18, with the following paragraph.

As interconnection density and integrated circuit density increase in semiconductor devices, the spacing between adjacent conductors decreases. As the spacing between adjacent conductors decreases, there is a corresponding increase in coupling capacitance (or mutual capacitance) between conductors. Adjacent conductors that exhibit a coupling or mutual capacitance form what is called a parasitic capacitor. In a typical integrated circuit device, parasitic capacitors are physically distributed over an integrated circuit and affect electrical operations therein. As the spacing between adjacent conductors decreases, the capacitance value of parasitic capacitors in an integrated circuit increases. Further, the topological widths of interconnections are decreased as circuit density is increased, causing an increase in the resistance of the interconnection.

IN THE CLAIMS

Amend the claims as follow

1. (Once amended) A method for fabricating a semiconductor device, comprising:

forming a conductive region on a substrate;